A Digital Phase Locked Loop Based Signal And Symbol Recovery System For Wireless Channel Signals And Communication Technology

Phase-Locked Loops for Wireless Communications: Digital, Analog and Optical Implementations, Second Edition presents a complete tutorial of phase-locked loops from analog implementations to digital and optical designs. The text establishes a thorough foundation of continuous-time analysis techniques and maintains a consistent notation as discrete-time and non-uniform sampling are presented. New to this edition is a complete treatment of charge pumps and the complementary sequential phase detector. Another important change is the increased use of MATLAB®, implemented to provide more familiar graphics and reader-derived phase-locked loop simulation. Frequency synthesizers and digital divider analysis/techniques have been added to this second edition. Perhaps most distinctive is the chapter on optical phase-locked loops that begins with sections discussing components such as lasers and photodetectors and finishing with homodyne and heterodyne loops. Starting with a historical overview, presenting analog, digital, and optical PLLs, discussing phase noise analysis, and including circuits/algorithms for data synchronization, this volume contains new techniques being used in this field. Highlights of the Second Edition: Development of phase-locked loops from analog to digital and optical, with consistent notation throughout; Expanded coverage of the loop filters used to design second and third order PLLs; Design examples on delay-locked loops used to synchronize circuits on CPUs and ASICS; New material on digital dividers that dominate a frequency synthesizer’s noise floor. Techniques to analytically estimate the phase noise of a divider; Presentation of optical phase-locked loops with primers on the optical components and fundamentals of optical mixing; Section on automatic frequency control to provide frequency-locking of the lasers instead of phase-locking; Presentation of charge pumps, counters, and delay-locked loops. The Second Edition includes the essential topics needed by wireless, optics, and the traditional phase-locked loop specialists to design circuits and software algorithms. All of the material has been updated throughout the book.

Digital Phase-locked Loops for Multi-GHz Clock Generation

The book reports two approaches of implementation of the essential components of a Digital Phase Locked Loop based system for dealing with wireless channels showing Nakagami-m fading. It is mostly observed in mobile communication. In the first approach, the structure of a Digital phase locked loop (DPLL) based on Zero Crossing (ZC) algorithm is proposed. In a modified form, the structure of a DPLL based systems for dealing with Nakagami-m fading based on Least Square Polynomial Fitting Filter is proposed, which operates at moderate sampling frequencies. A sixth order Least
Square Polynomial Fitting (LSPF) block and Roots Approximator (RA) for better phase-frequency detection has been implemented as a replacement of Phase Frequency Detector (PFD) and Loop Filter (LF) of a traditional DPLL, which has helped to attain optimum performance of DPLL. The results of simulation of the proposed DPLL with Nakagami-m fading and QPSK modulation is discussed in detail which shows that the proposed method provides better performance than existing systems of similar type.

BURSTLOCK is a digital phase-locked loop implemented using Burst Processing. It is used in a receiver perform FM demodulation of commercial broadcast signals. It is also shown that BURSTLOCK has some theoretical advantages over conventional phase-locked loops. (Author).

This book is intended for the graduate or advanced undergraduate engineer. The primary motivation for writing the text was to present a complete tutorial of phase-locked loops with a consistent notation. As such, it can serve as a textbook in formal classroom instruction, or as a self-study guide for the practicing engineer. A former colleague, Kevin Kreitzer, had suggested that I write a text, with an emphasis on digital phase-locked loops. As modem designers, we were continually receiving requests from other engineers asking for a definitive reference on digital phase-locked loops. There are several good papers in the literature, but there was not a good textbook for either classroom or self-paced study. From my own experience in designing low phase noise synthesizers, I also knew that third-order analog loop design was omitted from most texts. With those requirements, the material in the text seemed to flow naturally. Chapter 1 is the early history of phase-locked loops. I believe that historical knowledge can provide insight to the development and progress of a field, and phase-locked loops are no exception. As discussed in Chapter 1, consumer electronics (color television) prompted a rapid growth in phase-locked loop theory and applications, much like the wireless communications growth today. xiv Preface Although all-analog phase-locked loops are becoming rare, the continuous time nature of analog loops allows a good introduction to phase-locked loop theory.

The digital loop filter for an all-digital phase-locked loop was designed to meet a given set of specifications, and the performance of the filter was verified using MATLAB simulations. The number of bits used to represent each coefficients was selected so that the filter met specifications for magnitude while managing the are and power of the filter.

A systematic design procedure for a second-order digital phase-locked loop with a linear phase detector is proposed. The design procedure is based on the analogy between a type-II second-order analog PLL and a digital PLL. A new digital PLL architecture featuring a linear phase detector which eliminates the noise-bandwidth tradeoff is presented. It employs a stochastic time-to-digital converter (STDC) and a high frequency delta-sigma dithering to achieve a wide PLL bandwidth and a low jitter. The measured results obtained from the prototype chip demonstrate a significant jitter
All Digital Phase Locked Loops (ADPLLs) have become more attractive because they yield better testability, programmability, stability, and portability over different processes and the ADPLLs can reduce the system turn around time. Phase-locked loop mechanisms may be implemented as either analog or digital circuits. Both implementations use the same basic structure. The implemented ADPLL has two operation modes which are frequency acquisition mode and phase acquisition mode. In frequency acquisition mode, the ADPLL achieves a fast frequency locking via the proposed feed-forward compensation algorithm. In phase acquisition mode, the ADPLL achieves a finer phase locking.

Abstract: In this thesis a Full Digital Phase Locked Loop is designed and implemented in 0.13um technology node from TSMC. This full digital PLL is more advantageous than a traditional analog PLL because it eliminates the need for very fine analog voltage generated in a charge pump and it can be process independent. The focus of this thesis is to design and analyze a Digital Phase Locked Loop. This PLL has a lock range of 108MHz to 770MHz. A seven stage numerically controlled oscillator is implemented. Each inverter in the ring oscillator is driven by 21 tri-state inverters in parallel. To enable frequency control a 7 bit control word is decoded to enable these tri-state inverters. A second order integrating filter is used to average phase error and is clocked by control signals generated by a modified Phase Frequency Detector. This Full Digital PLL consumes 2.76mW of power when locked on at 720MHz.

A controller for an all digital phase locked loop which operates by pulse addition and removal is investigated. Being a first order system, the digital phase locked loop is more limited in regard to parameter controls than its second order analog counterpart. A loop with a fast lock time generally has poor phase/frequency accuracy, while a loop programmed for high accuracy will have slow lock time. Given that the digital phase locked loop is digitally programmable, a set of parameters may be selected which will minimize the lock time of the loop. Once the loop is locked, the parameters may be changed to alter the loop bandwidth and increase the loop accuracy. A controller circuit has been designed to adjust loop parameters in such a manner thereby optimizing loop performance. The exclusive-OR phase detector which is commonly used with the pulse addition/removal type digital phase locked loop has a phase lock range of plus or minus a quarter of a cycle. This work investigates the loop response to an incoming signal which is outside of the phase lock range of phase detector and inside the frequency lock range of the loop. A sub-circuit is proposed to improve the lock time of the loop when it encounters an incoming signal with these characteristics. The proposed circuits were designed using integrated circuit layout tools and submitted to a semiconductor manufacturer for fabrication. The controller concept and results of simulations and prototype experiments are presented.

Describes the implementation of a digital phase-locked loop for a demultiplexer application in which a pilot tone must be isolated at the receiver. The application relates to the receiving of telemetry signals from sonobuoys via a frequency modulated radio link. The implementation is on a vector processing card for real-time operation, with an automatic gain control placed in front of the digital phase-locked loop. Non-linear and linear models of the loop are also presented.

Phase Locked Loops (PLLs) are electronic circuits used for frequency control. Anything using radio waves, from simple radios and cell
phones to sophisticated military communications gear uses PLLs. The communications industry’s big move into wireless in the past two years has made this mature topic red hot again. The fifth edition of this classic circuit reference comes complete with extremely valuable PLL design software written by Dr. Best. The software alone is worth many times the price of the book. The new edition also includes new chapters on frequency synthesis, CAD for PLLs, mixed-signal PLLs, and a completely new collection of sample communications applications.